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Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks Chen Zhang1  
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## **Optimizing FPGA-based Accelerator Design for Deep**

This page contains the complete set of materials for my FPGA & Verilog design course which I taught in Isfahan University of Technology, 2010.

## **FPGA & Verilog Design – Mohammad S. Sadri - Googoolia**

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Spartan-6 FPGA PCB Design and Pin Planning www.xilinx.com UG393 (v1.3) October 17, 2012 Xilinx is disclosing this user guide, manual, release note, and/ or ...

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## **Field-programmable gate array - Wikipedia**

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## **Graphical/Text Design Entry - FPGA Design - Solutions - Aldec**

This community-based site is dedicated to helping you jump-start your design with the Xilinx Zynq®-7000 All Programmable SoCs and UltraScale+ MPSoCs.

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## **Embedded Design Handbook - intel.com**

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### **Lattice Diamond - Lattice Semiconductor**

Yesterday at Hot Chips 29 (2017) I presented a poster GRVI Phalanx: A Massively Parallel RISC-V FPGA Accelerator Framework: A 1680-core, 26 MB SRAM Parallel Processor ...

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### **Software Defined Radio (SDR) OMAPL-138-based Hardware**

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### **Papilio DUO Hardware Guide - Papilio FPGA Platform**

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